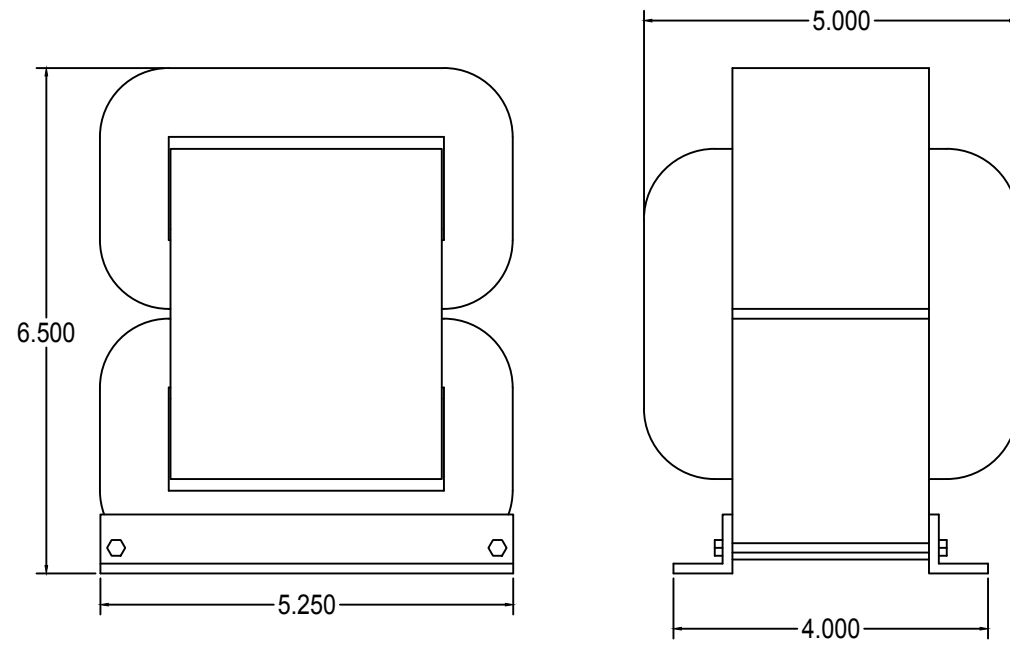
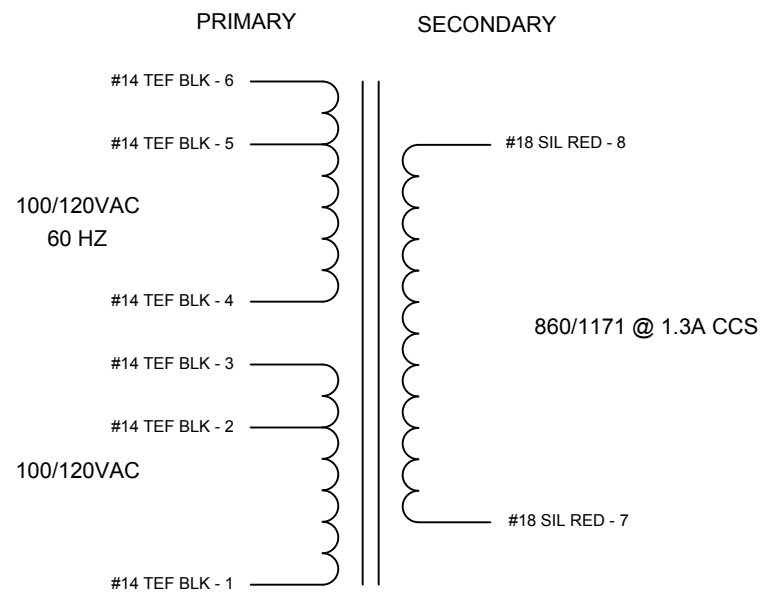
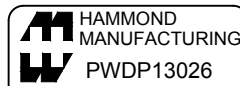


SCHEMATIC DIAGRAM

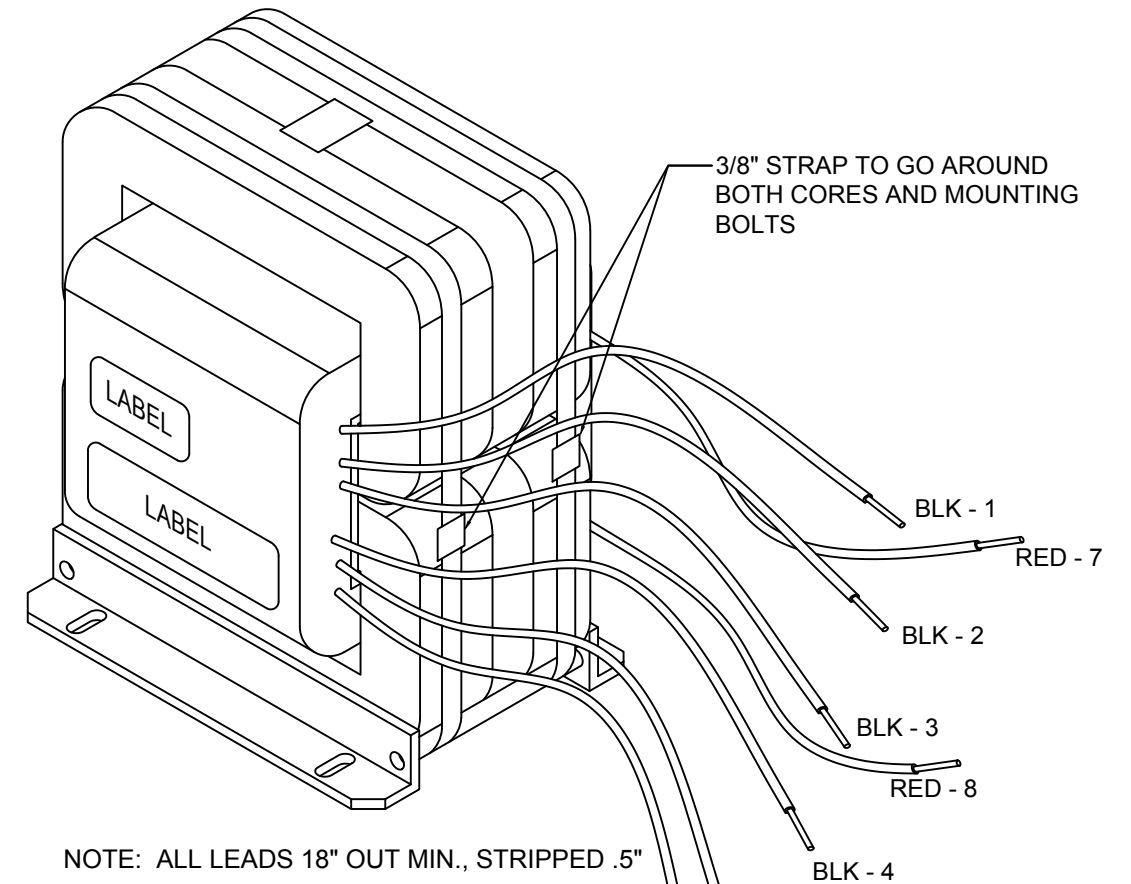


WIRES NOT SHOWN IN THIS VIEW

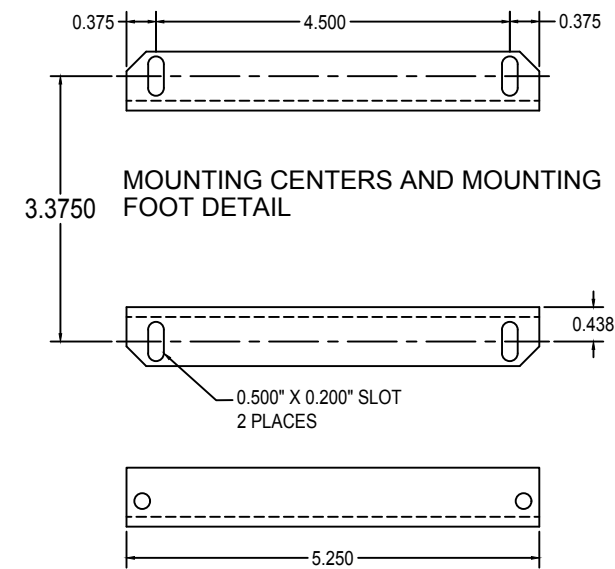


PRIMARY - 117V
INPUT LEADS 1 & 2
JUMPER 1 TO 4 & 2 TO 5
OUTPUT 7 - 8 1171V
INPUT LEADS 1 & 3
JUMPER 1 TO 4 & 3 TO 6
OUTPUT 7 - 8 860V

PRIMARY - 234V
INPUT LEADS 1 & 5
JUMPER 2 TO 4
OUTPUT 7 - 8 1171V
INPUT LEADS 1 & 6
JUMPER 3 TO 4
OUTPUT 7 - 8 860V



NOTE: ALL LEADS 18" OUT MIN., STRIPPED .5"



ELECTRICAL DATA:

TESTS	CONDITIONS	ACCEPTANCE CRITERIA
SEC N.L.V.	@117V INPUT 1 - 2, JUMPER 1 TO 4 AND 2 TO 5	7 TO 8 = 1183V ±2%
	@117V INPUT 1 - 3, JUMPER 1 TO 4 AND 3 TO 6	7 TO 8 = 887V ±2%
	@234V INPUT 1 - 5, JUMPER 2 TO 4	7 TO 8 = 1183V ±2%
	@234V INPUT 1 - 6, JUMPER 3 TO 4	7 TO 8 = 887V ±2%
DCR	1 - 3 =	0.258 ±20%
IN OHMS	4 - 6 =	0.300 ±20%
	7 - 8 =	13.8 ±20%
HIPOT	PRIMARY - CORE	3500V, 60Hz, 1 SEC
	SEC - CORE	7000V, 60Hz, 1 SEC
	PRI - SEC	7000V, 60Hz, 1 SEC
	PRI - PRI	3500V, 60Hz, 1 SEC

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REV	NOTES	BY	DATE	REV	NOTES	BY	DATE
1	CORRECTED DIMENSION TABLE	CB	05/07/14				
2	REVISED MOUNTING BRACKET	CB	06/19/14				
3	REVISED MOUNTING BRACKET	CB	06/25/14				
4	CORRECT VOLTAGE ON TABLE	CB	06/13/19				

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EDB PWDP13026

DRAWN CBACIK	DATE 05/23/14	NUMBER PWDP13026
APPROVED	DATE	